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Application of computational fluid dynamics simulation tools for thermal characterization of electronic packages

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Abstract

Purpose – In the semiconductor electronics industry, effective heat removal from the integrated circuits (IC) chip, through the electronic package to the environment is crucial to maintain an allowable junction temperature of the IC chip. Thermal performances of such electronic packages are characterized by package thermal resistance called θ-JA and are widely used in the electronic industry. Improving thermal performance is numerically predicted using computational fluid dynamics (CFD) technique and experimental tests are carried out to verify the numerical predictions. To provide new/additional data and demonstrate CFD technique for thermal characterization of electronic packages with experimental results.

Design/methodology/approach – The thermal performance of electronic packages has been studied using a CFD technique. The finite volume method is a technique used for solving a set of partial differential equations in a domain, using control volume based discretization. A detailed thermal model of an electronic package was created using a CFD tool and validated against the experimental data obtained in a natural convection environment, compliant to JEDEC standards. The thermal performance of the package was evaluated for different die sizes and epoxy molding compounds at different power levels. The use of a heat slug was investigated to identify its effect on heat dissipation for the future generations of IC, which are expected to be smaller in size and to dissipate more power. Free convective flow velocities, detailed temperature and heat flow distributions around the package will also be presented.

Findings – The study demonstrates that applying CFD techniques can provide accurate results on estimating thermal characterization of an electronic package. Predicted device junction temperatures as well as the thermal resistance of packages can be predicted with a good accuracy for different ranges of power levels in natural convection. The numerically estimated die junction temperatures have also been found to be accurate and reliable.

Research limitations/implications – The analysis is limited to an incompressible fluid. The effect of forced convection is not considered.

Practical implications – New and additional generated data will be helpful in the design and decision making time of the product to choose a low cost and viable thermal performance solution in the cooling of electronic components at low power.

Originality/value – The electronic package involves multi-material and applying CFD technique is useful to determine the accurate thermal performance and simple and fast to apply for different conditions/material sets. Predictions of junction-to-ambient thermal resistance and device junction temperature values are compared against measurements. Excellent correlation was obtained. The results thus obtained compare well with the experimental results, but the computational effort and time required in the analysis is much small as compared.

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Paper type Technical paper

Introduction

Technological enhancements at device, package, and system levels have resulted in increased functionality and decreased form factors. As a consequence, thermal management has become more critical and a thermal analysis must be included early in the design cycle for handheld electronics and communication products, such as cellular phones, digital cameras, personal digital assistants (PDA).

The majority of integrated circuits (IC) operates best within a limited temperature range and their packages are expected to remove excessive heat. Furthermore, a high operational junction temperature decreases device reliability and reduces the operating lifetime of the device. In some specific applications, such as digital cameras, high junction temperatures will also directly impact the component performance, like image quality. Some handheld products dissipate low power (milliwatts) but during very short periods of time. Therefore, an understanding of the package thermal performance is necessary even for these devices.

A non-standard, unsymmetrical custom-made plastic quad flat package (PQFP) is considered a potential solution for upcoming products, provided the thermal requirements can be met. Considering that future generation ICs may be 40-60 percent smaller than the existing devices and are estimated to dissipate 30-50 percent more power, a study has been conducted to find ways to enhance the thermal performance of this low cost PQFP package.

The thermal performance of electronic packages generally is quantified in terms of the thermal resistance. JEDEC has published standards (EIA/JEDEC Standard, JESD-51-2, 1995a; EIA/JEDEC Standard, JESD-51-1, 1995b) to define test methods and guidelines to determine the thermal resistance. The measurement of junction temperature at a given set of environmental conditions and various levels of power dissipation is a common approach. Thermal performance of the packages has been widely investigated using the experimental and numerical methods. In the latter case, several techniques, such as conduction based simulation models, thermal resistance network compact models and genetic approaches, are used by Sarang *et al.* (1999) to predict the thermal performance of electronic packages and the die junction temperature. A conduction based simulation model has the severe limitation that empirically determined convective heat transfer coefficients (HTC) are applied on different exposed surfaces (Teoh *et al.*, 2000). Some investigators have made an attempt using an evolutionary genetic approach for solving heat transfer problems in electronic packages (Parthiban *et al.*, 2000). Sometimes second level assembly boards are not accounted for, eventually resulting in inaccurate thermal predictions.

Recently, there is a tremendous increase in the use of conjugate heat transfer models (Burgos *et al.*, 1995), which are solved using well-developed methods of computational fluid dynamics (CFD). In conjugate analysis, heat conduction in the solids is simultaneously solved with the fluid flow and heat transfer in the cooling medium. A CFD-based technique has a distinct advantage of solving momentum and energy equations to predict thermal performance of the electronic device thus minimizing the number of assumptions. This technique was originally developed for aerospace applications and has a vital role in electronics thermal management. It also helps to

identify and optimize viable thermal solutions early in the design cycle with reduced product development iterations. Numerical predictions are validated by measuring the package junction to ambient thermal resistance (θ_{JA}) and device junction temperature (T_j) by the well-known electrical test methods (EIA/JEDEC Standard, JESD-51-2, 1995a; John, 1997). The advantage of an electrical test method over other temperature measurement techniques such as liquid crystal (Teoh *et al.*, 2000; Azar and Dino, 1997) and infrared measurement methods is that no surface treatment is required.

The thermal performance of a PQFP package will be presented in this paper. A parametric study has been executed to understand the effects of chip junction temperatures at two different die sizes, varying power levels, three different molding compounds and at different ambient temperatures in a natural convection environment. This study also examined the effects of heat slugs on the thermal resistance.

Thermal modeling and CFD solution

Problem descriptions and thermal model

A PQFP package was mounted on a two-layer board (one layer for signals and the other layer for power) and the whole assembly was placed horizontally in a plexiglas, still air enclosure with a volume of one cubical foot, as recommended by the JEDEC standard (Figure 1).

A detailed thermal model of the package was created using FLOTHERM®, a commercially available CFD tool. This tool uses a finite volume method for solving the conservation equations for mass, momentum and energy. It is based on non-linear partial differential equations for fluid flows and heat transfer predictions. Three-dimensional governing equations are solved for steady state solutions inside the enclosure around the package.

Figure 2 shows the heat slug located on the bottom of the die flag in the PQFP package. This heat slug is attached to the second level PCB board using thermally conductive epoxy. The structural items of the package thermal model include the die, the die attach epoxy, the die flag, the tie bars, the heat slug, the lead frame and the plastic epoxy molding compound. These components have been modeled as a series of embedded conductive cuboidal blocks. The thermal conductivity of each material is listed in Table I.

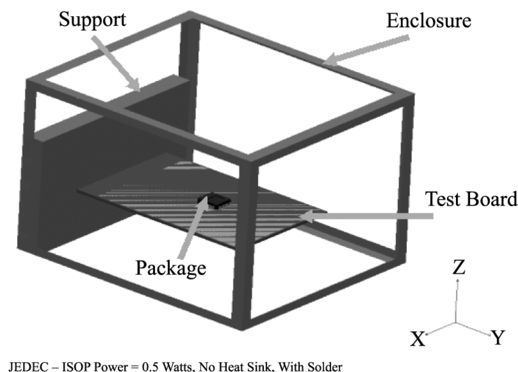


Figure 1.
Test board with package inside JEDEC enclosure

Governing equation

Numerical modeling of practical situations inside a system domain involves fluid flow, heat transfer, mass transfer, turbulence and other related phenomena. These phenomena are governed by the principles of conservation of mass, momentum and energy. The relations are expressed as partial differential equations, which possess a common form. The recognition of this common form provides a major convenience for the construction of the numerical procedure. This common relation is expressed in rectangular Cartesian coordinates as:

$$\frac{\partial}{\partial t}(\rho\phi) + \mathrm{div}(\rho\vec{V}\phi - \Gamma_\phi \,\mathrm{grad}\,\phi) = S_\phi \tag{1}$$

$$\text{Transient} + \text{Convection} - \text{Diffusion} = \text{Source}$$

where ρ is the density, $\vec{V}$ the velocity vector, ϕ the dependent variable (fluid velocities are u, v and w in the X, Y and Z directions), Γ_ϕ the diffusion coefficient (laminar plus turbulent) and S_ϕ the source or sink term. To obtain mass conservation, equate $\phi = 1$. For momentum conservation, equate $\phi = u$. For energy conservation, equate $\phi = T$ with T representing temperature. Finally, Γ_ϕ represents transport properties such as viscosity or conductivity, which, in conjunction with the gradient of appropriate dependent variable, leads to the diffusion flux such as viscous stress or heat flux. The source term is meant primarily for heat generation in a fluid and the generation of turbulence kinetic energy. When the corresponding physical quantity is absorbed rather than produced, the source term becomes a sink. Source terms are pressure gradient, body forces and any contribution from viscous terms that is not accommodated in the diffusion term.

Numerical method and boundary conditions

The finite volume method is a technique used for solving a set of partial differential equations in a domain, using control volume based discretization. The governing partial differential equations from the conservation equations usually result in coupled

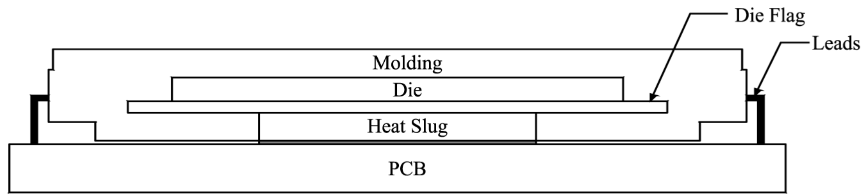


Figure 2.
Thermal model of PQFP package (side view)

Table I.
Component thermal properties

Material	Thermal conductivity k (W/m K)
Molding compound	0.6
Silicon die	$117.5 - 0.42\,(T - 100)$
Die attach epoxy	4.5
Leads	259.8
Heat slug	259.8
PCB dielectric	0.30

set of algebraic equations. Solutions of such systems of equations are obtained in a segregated manner using the SIMPLE algorithm (Patankar, 1980). The finite volume technique and its solution procedure can also be found in Versteeg and Malalasekera (1995). Each individual system of equations is solved iteratively until convergence. The solution is assumed converged when the maximum temperature and velocity (T, u, v, and w) change during successive iterations is less than 1×10^{-3} percent. Thermal behavior has been simulated in natural and forced convection environments. Radiative heat transfer mechanisms have been included. The domain of integration was not extended to the boundaries of the enclosure box. Instead the domain extended 2 mm below the board, 50 mm above the board and in a similar manner from the sides of the board. A direct benefit of this choice is that the computational grid is used entirely to focus on the resolution of the boundary layers around the board and the package.

At the boundaries of the domain, free air conditions are applied, fixing the relative pressure to zero with any incoming air entering with the prescribed ambient temperature. This way bulk heating of the air within the enclosure as a whole is restricted. A partial grid refinement study was conducted by evaluating progressively finer grid sizes. A structured grid is generated with manual control using grid patch technique. The fine grid employed was $115 \times 127 \times 73$ (over one million) cells. The computation takes around 8-9 h for each run on a HP Kayak XU 800 PC with dual processor and 512 MB RAM. The model is not symmetric, therefore full 3D model of the problem is considered. This choice significantly increases the computational time needed to solve for airflow velocities, pressure and temperature.

The airflow generated inside the domain for natural convection is assumed to be laminar and to have a maximum velocity of approximately 0.1 m/s. The benefit of using CFD is that the local HTC across the surface of the package and board are calculated automatically. If the flow is fully laminar these values come directly from the solution of the governing equations itself. Whereas for turbulent flow, the CFD method uses well established wall models to derive the local HTC.

Methodology of thermal measurement

The electrical test method was used for junction temperature measurement. This method is a direct, non-contact technique as it utilizes the junction itself as the temperature sensor, i.e. the temperature and voltage dependency exhibited by all semiconductor diode junctions. The equipment used for thermal measurement meets the requirement as per JEDEC specification (EIA/JEDEC Standard, JESD-51-2, 1995a; EIA/JEDEC Standard, JESD-51-1, 1995b). The measurement setup includes a one cubic foot JEDEC enclosure, thermal analyzer and an external DC power supply.

The measurement procedure comprises two steps: device calibration and actual measurement. Device calibration is the procedure for determining the calibration parameters of slope and temperature intercept. The voltage generated in response to the applied sense current is used to compute the junction temperature using the calibration relationship. These measurements are performed under unpowered, thermal equilibrium conditions so that the junction and case temperature are nearly equal. V_{f} is the diode forward biased voltage (V) that is usually taken as the temperature sensitive parameter (TSP) for measuring the junction temperature of the device. The device diode forward voltage versus junction temperature can then be expressed mathematically in linear equations as given below:

$$T_j = mV_f + T_o \qquad (2)$$

where T_j is the junction temperature of the device (°C), m the slope (°C/V), and T_o the temperature ordinate intercept (°C). The device was recalibrated to adjust for part-to-part variations by using a single temperature-voltage data point during the actual measurement. After recalibration, the steady state junction-to-ambient thermal resistance was measured using the calibrated TSP relationship between the device voltage and junction temperature. The package was powered by passing the heating current via the regulated power supply across the diode. When the thermal equilibrium is reached, diode voltage and the enclosure ambient temperature are recorded and junction temperature at that forward voltage is determined from the calibration parameters. The analyzer performs these steps automatically. Subsequently, the junction to ambient thermal resistance, θ_{ja} (°C/W), is calculated automatically by a thermal analyzer using the following equation:

$$\theta_{ja} = \frac{T_j - T_a}{P} \qquad (3)$$

here T_a represents the ambient temperature (°C), and P the power dissipation of the die in watts. Ten test boards have been made of FR-4 material. The thickness of the copper traces is compliant to the JEDEC standards (EIA/JEDEC Standard, JESD 51-7, 1999; EIA/JEDEC Standard, JESD-51-3, 1996).

Results and discussion

Flow pattern and temperature distribution

The package thermal resistance and the die junction temperature have been evaluated at different power ranges with ambient temperatures of 25 and 45°C. A uniform heat input varying between 100 and 1,000 mW was placed on the mid-region of the die. Experiments have been performed to validate the numerical predictions at an ambient temperature of 25°C only.

The dissipated power initiates a thermal plume rising from the package as shown in Figure 3. The maximum airflow vector was found to measure 0.08 m/s in natural convection. The weak flow is generated by the buoyancy effect. The thermal contours in the *X-Z* plane are shown in Figure 4 for natural convection.

The temperature contours for a package with heat slug and a package without heat slug in natural convection are shown in Figure 5. The location of the maximum temperature at the centerline corresponds to the center of the die heat source. The average device junction temperature of a die (which will henceforth be referred to as Die A) for a package without heat slug was predicted to be 13.4°C above an ambient temperature of 45°C at the center of the die with a power of 200 mW. The device junction temperature drops already by 1.5°C at low power levels if a heat slug is used. The temperature contours shown in Figure 5 reveal that more heat tends to flow through the PCB in case a heat slug is placed on the bottom of the die. Figure 6 shows the temperature contour patterns on the horizontal *X-Y* plane in the middle of the test board. These contours have been found to be circular symmetric.

The heat transfer rate as extracted from the numerical simulations in still air at a typical power dissipation of 200 mW is shown in Table II. Approximately, 170 mW

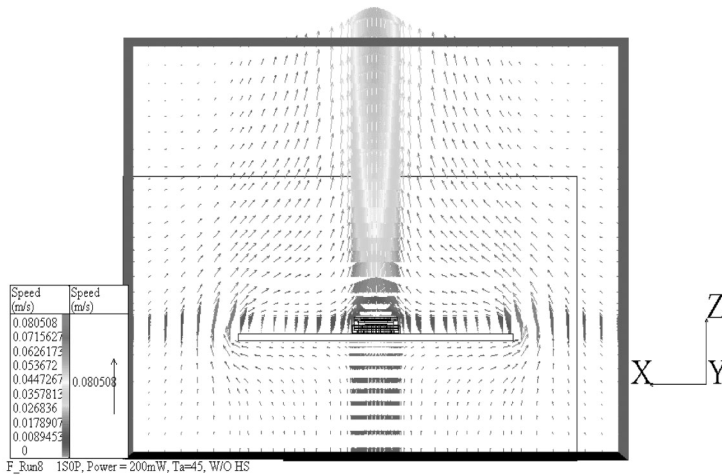


Figure 3.
Typical flow vectors (X-Z plane)

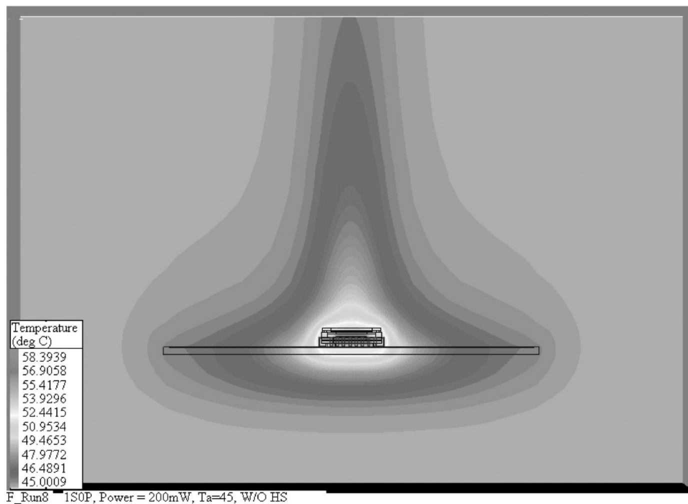
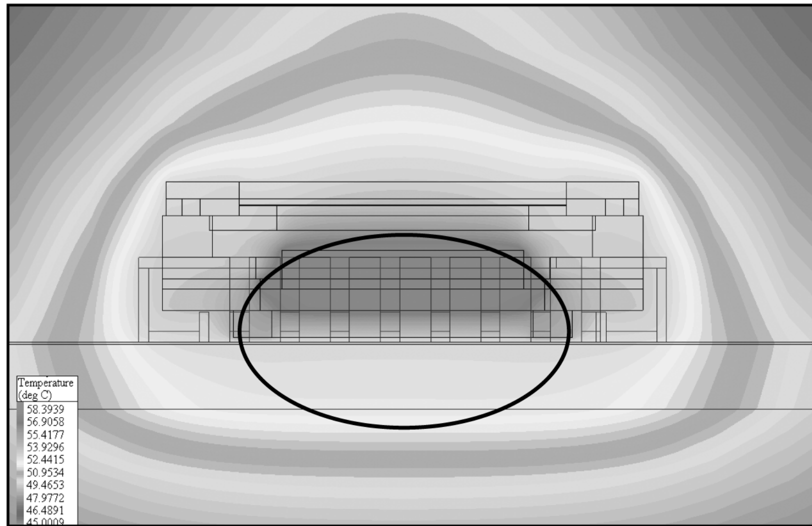


Figure 4.
Temperature distribution (X-Z plane)

(85 percent) enters the test board through the leads and the bottom of the package. The remaining heat is being dissipated through the top and sides of the package. Evidently, the board acts as a heat sink. Clearly, the still air measurement is a characterization of the board-package assembly rather than the package alone.

Results of thermal resistance

The numerical predictions of the thermal resistance for Die A are compared against the measured data shown in Figure 7 for packages with and without heat slug. After several corrections and with an increased number of grid cells (>1.0 million),



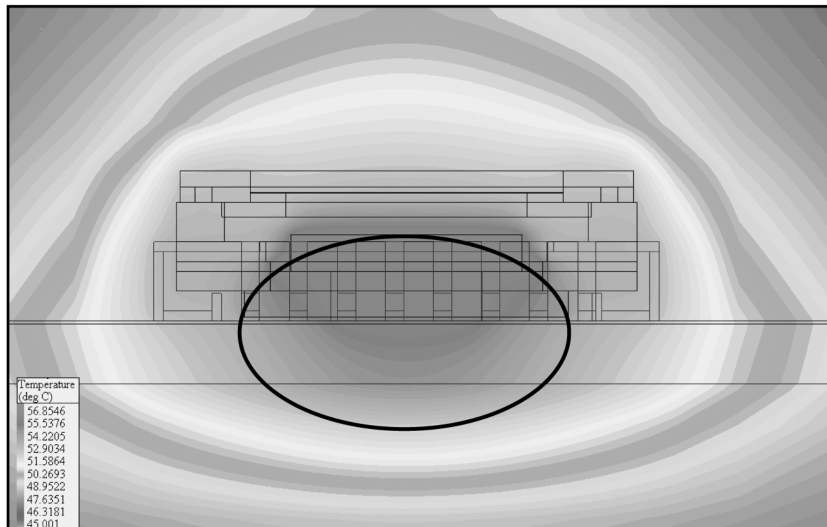


Figure 5.
Typical temperature distribution around the package in the *X-Z* plane

the differences between the numerical predictions and measurements were found to be smaller than 20 percent. Furthermore, it was found that the thermal resistance decreases by approximately 7.2°C/W or 10 percent as a result of the introduction of a heat slug.

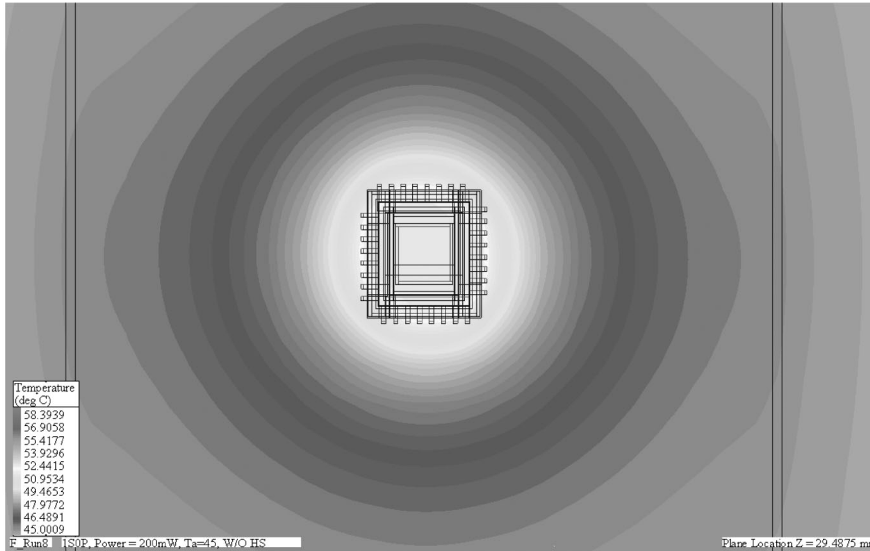


Figure 6.
Flow vectors inside the enclosure in the *X-Z* plane

Table II.
Thermal budget for PQFP package without heat slug

Heat flow	Relative percentage
Package top	12.3
Package sides	2.5
Package bottom	85.2

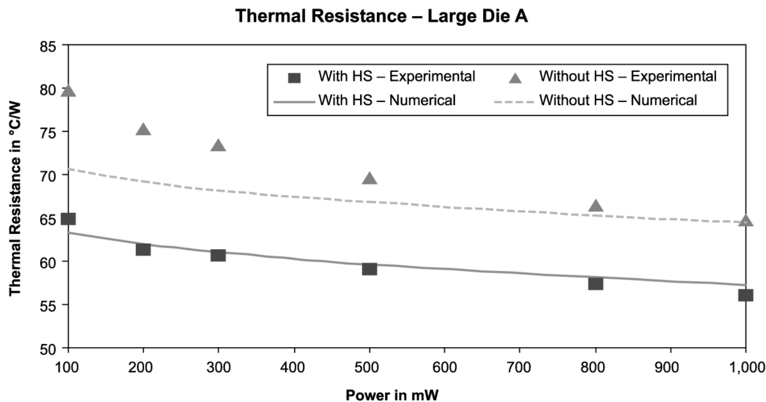


Figure 7.
Comparison of thermal resistance with and without heat slug

At a certain low power level the difference between the predicted thermal resistance and measurement was found to be 11.4 percent for a package without heat slug. At a certain high power lower level this difference reduces to 3.0 percent. It should be noted that the predictions for a package with a heat slug match the measured values.

The effect of die size on junction temperature and thermal resistance

Two different die sizes have been analyzed (Die A and Die B). The surface area ratio of Die B to Die A is estimated to be 0.45 and the thickness of both dies has been considered to be identical. A comparison of maximum device junction temperatures and package thermal resistance values with and without heat slug between larger and smaller dies is shown in Figure 8. A thermal analysis has been executed at an ambient temperature of 25°C with an IC power dissipation of 500 mW. Decreasing the die size by 50 percent did not introduce a significant change in the device junction temperature (1 percent only). The use of a heat slug reduces the device junction temperature by 4°C. Thermal resistance values are predicted to be higher (by 7.2-7.9°C/W or 10-12 percent) for the smaller Die B as compared to Die A.

Junction temperature and thermal resistance values have been found to be in excellent agreement with the experimental tests at power dissipation levels around 500 mW. This agreement can be explained by the fact that the measurements in a natural convective flow are more stable at high power levels, as considered for this study.

The effect of different EMC on package thermal resistance

Three different types of EMC were considered for the study (EMC-A, EMC-D and EMC-F). The thermal conductivity of EMC-D measured 3 percent of that of EMC-A whereas the thermal conductivity of EMC-F measured 0.8 percent of that of EMC-A. The thermal resistance values for these EMCs at different power levels in still air are shown in Figure 9. It can be concluded that the use of EMC-A will reduce the thermal resistance by 37 percent as compared to EMC-F and 21 percent as compared to EMC-D. EMC-D offers an improvement of 18 percent as compared to EMC-F in terms of thermal resistance. In conclusion, the effect of changing the EMC was found to be more significant than that of adding a heat slug.

Conclusions

The study presented in this paper demonstrates that an accurate thermal model of a PQFP package can be obtained by a CFD technique. Device junction temperatures as well as the thermal resistance of packages can be predicted with a good accuracy for

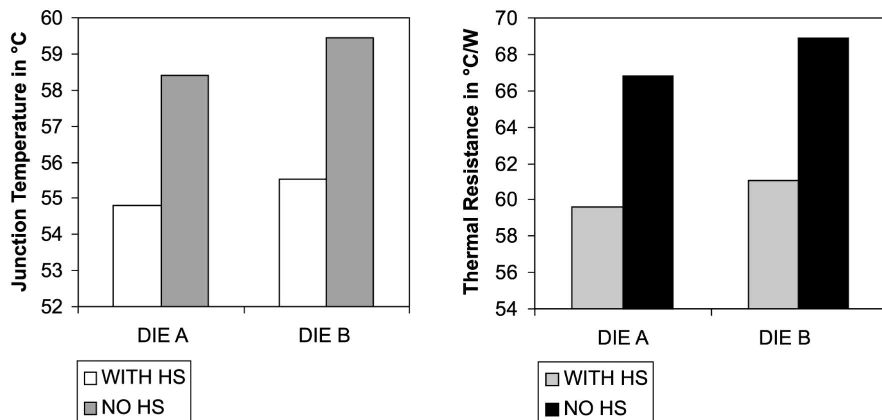


Figure 8.
Comparison of the junction temperature and the thermal resistance of two dies (Die B being 50 percent smaller than Die A)

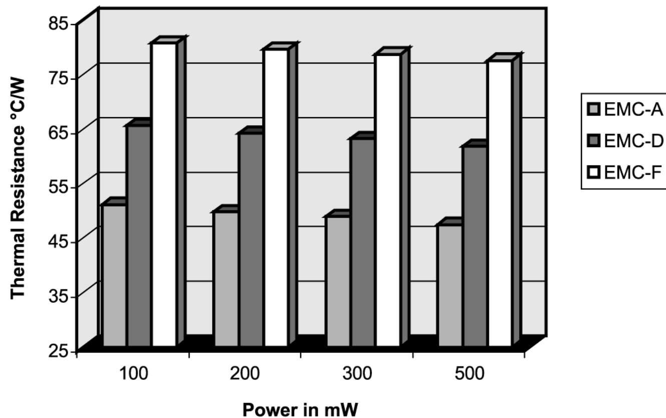


Figure 9.
Comparison of the thermal resistance of various epoxy molding compounds

different ranges of power levels in natural convection. The numerically estimated die junction temperatures have also been found to be accurate and reliable: the differences against measured data are less than 15 percent. The package thermal resistance with and without heat slug has been predicted with good accuracy in natural convection environments. The effect of adding a heat slug on the thermal performance has been found to be less significant than the effect of EMC selection. The latter can be as high as over 35 percent in terms of thermal resistance.

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